## *Remarks*

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-30, 32-47, and 49-51 are pending in the application, with claims 1, 16, 29, 33, 35, 37, 39, 44, 49, and 50 being the independent claims. Claims 1, 5, 16, 29, 33, 35, 39, 44, 49, and 50 are sought to be amended. Claims 31 and 48 are sought to be canceled without prejudice to or disclaimer of the subject matter therein. Claim 52 is sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

### *Allowable Subject Matter*

Applicants acknowledge with appreciation the Examiner's indication that claims 37 and 38 are allowed and claims 5, 20, 23, 26, 27, 30-32, 40, 48, and 51 would be allowable if rewritten in independent form including all of the limitations of their base claim and any intervening claims.

### *Rejections under 35 U.S.C. § 102*

Kim

In the Office Action, claim 29 was rejected under 35 U.S.C. §102(e) as being anticipated by Kim, U.S. Patent No. 6,7744,319 (Kim). Claim 29 has been amended to incorporate the subject matter of allowable dependent claim 31. Applicants respectfully

submit that amended claim 29 is therefore allowable. Reconsideration and withdrawal of this rejection is therefore respectfully requested.

Yamamoto

In the Office Action, claims 33-36 were rejected under 35 U.S.C. §102(e) as being anticipated by Yamamoto, U.S. Patent No. 6,552,611 (Yamamoto). Applicants respectfully traverse this rejection.

Yamamoto describes a differential amplifier including a first differential circuit 17 composed of transistors M41, M42, and M43 and a second differential circuit 18 composed of transistors M44, M45, and M46. (Yamamoto, FIG. 9, col. 11, lines 50-53). A first resistance Ro1 and a second resistance Ro2 are connected as loads to the current output terminals 21 and 22 of the circuit, respectively, which produces a voltage output. (Yamamoto, col. 13, lines 1-5).

Applicants submit that Yamamoto does not teach or suggest a transconductance cell having a "first feedback loop ... wherein the first feedback loop includes a first inverter stage, a first input transistor having a drain coupled to an input of the first inverter stage and a first output transistor having a gate coupled to an output of the first inverter stage, wherein the first feedback loop is configured to keep $V_{GS}$ of the first input transistor constant" and a " a second feedback loop ...wherein the second feedback loop includes a second inverter stage, a second input transistor having a drain coupled to an input of the first inverter stage and a first output transistor having a gate coupled to an output of the first inverter stage, wherein the second feedback loop is configured to keep $V_{GS}$ of the second input transistor constant," as recited in amended independent claims 33 and 35.

For at least the above reasons, amended independent claims 33 and 35 are patentable over Yamamoto. Furthermore, for at least the above reasons and further in view of their own features, claim 34 which depends from claim 33 and claim 36 which depends from claim 35 are patentable over Yamamoto. Reconsideration and withdrawal of this rejection is therefore respectfully requested.

Cyrusian

In the Office Action, claims 44-47 and 49 were rejected under 35 U.S.C. §102(e) as being anticipated by Cyrusian, *et al,* U.S. Patent No. 6,570,447 (Cyrusian). Applicants respectfully traverse this rejection.

Claim 44 has been amended to incorporate the subject matter of allowable dependent claim 48. Applicants respectfully submit that amended claim 44 is therefore allowable. For at least these reasons, and further in view of their own features, claims 45-47 which depend from claim 44 are patentable over Cyrusian. Reconsideration and withdrawal of this ground of rejection is therefore respectfully requested.

Claim 49 has been amended to depend from independent claim 39. Cyrusian does not overcome all the deficiencies of Akita or Wanlass relative to amended independent claims 39, described below. For at least these reasons, and further in view of its own features, dependent claim 49 is patentable. Reconsideration and withdrawal of this ground of rejection is therefore respectfully requested.

Hirano

In the Office Action, claim 50 was rejected under 35 U.S.C. §102(b) as being anticipated by Hirano, *et al,* U.S. Patent No. 5,179,298 (Hirano). Applicants respectfully traverse this rejection.

Hirano describes an input buffer circuit 1 having four inverter stages. (Hirano, FIG. 1). The input buffer circuit 1 "adjusts the resistance value between the NMOST and grounding voltage VSS, or the resistance value between the PMOST and supply voltage VCC, or both resistance values so as to decrease the current flowing from the supply voltage VCC to the grounding voltage VSS." (Hirano, Abstract). In support of this rejection, the Examiner equates the PMOS transistor in the second inverter stage (QP2), the third inverter stage (QP3, QN3), and PMOS transistor (QP4) in the fourth inverter stage to the feedback loop recited in Applicants' independent claim 50. Applicants' respectfully disagree with this understanding.

In the rejection, the Examiner is attempting to isolate the PMOS transistor in the second stage (QP2) and the PMOS transistor in the fourth stage (QP4) from their complementary NMOS transistors to achieve the subject matter recited in claim 50. However, transistor QP2 and transistor QP4 do not operate in isolation from QN2 and QN4. As discussed above, the invention in Hirano relies on the use of complementary transistors in each stage. When considered in the context of the entire input buffer circuit, transistor QP2, inverter stage (QP3, QN3), and transistor QP4 do not form a "feedback loop ... wherein the operation of the feedback loop causes $V_{GS}$ of the input transistor to remain substantially constant," as recited in amended claim 50. The

operation of inverter stage (QP3, QN3) and PMOS transistor QP4 do not substantially effect the operation of PMOS transistor QP2.

For at least the foregoing, amended independent claim 50 is patentable over Hirano. Reconsideration and withdrawal of this ground of rejection is therefore respectfully requested.

***Rejections under 35 U.S.C. § 103***

Akita and Wanlass

In the Office Action, claims 1-4, 7-19, 22, 24, 25, 28, 39, and 41-43 were rejected under 35 U.S.C. §103(a) as being rendered obvious by Akita, *et al,* U.S. Patent No. 4,080,828 (Akita) in view of Wanlass, *et al,* U.S. Patent No. 3,356,858 (Wanlass). Applicants respectfully traverse this rejection.

The combination of Akita and Wanlass does not teach or suggest all the elements of Applicants' amended independent claims 1, 16, and 39. Akita describes a liquid level detecting apparatus having a plurality of ring oscillators (210, 220, 230) connected in parallel. (Akita, FIG. 6). Each ring oscillator includes three inverter gates connected in series. The output of the third inverter gate is fed back through an inductor as the input of the first inverter gate, forming the ring. (Akita, FIG. 6). Wanlass describes an inverter circuit having a PMOS transistor and a complementary NMOS transistor. (Wanlass, FIG. 5, col. 4, lines 55-59).

Ring oscillators, such as described in Akita, generate a periodic signal. Applicants therefore submit that the combination of Akita and Wanlass does not teach or suggest a "first feedback loop ... wherein the operation of the first feedback loop causes $V_{GS}$ of the first input transistor to remain substantially constant" and a "second feedback

loop ... wherein the operation of the second feedback loop causes $V_{GS}$ of the second input transistor to remain substantially constant," as recited in amended independent claims 1, 16, and 39.

For at least the foregoing reasons, amended independent claims 1, 16, and 39 are patentable over the combination of Akita and Wanlass. Furthermore, for at least the above reasons and further in view of their own features, claims 2-4 and 7-15 which depend from claim 1, claims 17-19, 22, 24, 25, and 28 which depend from claim 16, and claims 41-43 which depend from claim 39 are patentable over the combination of Akita and Wanlass. Reconsideration and withdrawal of this ground of rejection is therefore respectfully requested.

Chau and Akita

In the Office Action, claims 1, 6, 16, and 21 were rejected under 35 U.S.C. §103(a) as being rendered obvious by Chau, *et al,* U.S. Patent No. 5,682,123 (Chau) in view of Akita. Applicants respectfully traverse this rejection.

The combination of Chau and Akita does not teach or suggest all the elements of Applicants' amended independent claims 1 and 16. Chau describes a voltage controlled oscillator having a current controlled oscillator formed of a loop of serially connected inverters. (Chau, FIG. 3, Abstract). To form the loop, the output of the last inverter is fed back as input to the first inverter.

Akita does not overcome all the deficiencies of Chau relative to amended independent claims 1 and 16. Ring oscillators, such as described in Chau and Akita, generate a period signal. Applicants therefore submit that the combination of Chau and Akita does not teach or suggest a "first feedback loop ... wherein the operation of the

first feedback loop causes $V_{GS}$ of the first input transistor to remain substantially constant" and a "second feedback loop ... wherein the operation of the second feedback loop causes $V_{GS}$ of the second input transistor to remain substantially constant," as recited in amended independent claims 1 and 16.

For at least the foregoing reasons, amended independent claims 1 and 16 are patentable over the combination of Chau and Akita. Furthermore, for at least the above reasons and further in view of their own features, claim 6 which depends from claim 1 and claim 21 which depends from claim 16 are patentable over the combination of Chau and Akita. Reconsideration and withdrawal of this ground of rejection is therefore respectfully requested.

## *Conclusion*

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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